Education on CMOS RF Circuit Reliability

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Abstract

This paper presents a design methodology to study RF circuit performance degradations due to hot carrier and soft breakdown. The experimental facts of DC stress on the RF properties of MOSFETs are given. The equivalent circuit model is developed and verified by measurement data. RF circuit such as a low noise amplifier is evaluated using SPICE circuit simulation. Noise figure and s-parameter degradations subject to hot electron stress and gate oxide breakdown are reported.

Introduction

Today’s electronics products in wireless communications require low power dissipation and longer lifetime of battery. Silicon CMOS is the key semiconductor technology to produce high-density integrated circuits with low power dissipation for portable electronics. High speed and high frequency operation of electronic systems and circuits are essential for data/voice transmission for the information age.

When CMOS device sizes are minimized to achieve high density, the channel electric field of MOS transistors becomes higher. This enhances hot carrier (HC) effects. Furthermore, the scaling of oxide thickness could trigger the gate oxide soft breakdown (SBD). As a result, reliability issues in CMOS devices and circuits become very important. Degradation of the DC device parameters has received widespread attention, but the degradation of RF circuit performance has not been studied and taught systematically.

In this paper, a systematic methodology to study RF circuit performance degradations due to HC and SBD effects is developed. The experimental facts of DC stress on the RF properties of MOSFETs are provided. The methodology to study the HC and SBD effects on RF circuits is proposed. The performance degradations of the two important RF circuits, a low noise amplifier and a voltage-controlled oscillator, are evaluated using the methodology developed. Furthermore, this talk stresses the importance of RF circuit education for the information age. For example, to present what students or engineers need to know beyond the traditional textbooks or teaching in integrated circuits design in engineering education.

Theoretical Understanding

Hot carriers are usually referred to damage of Si/Si interface state and charge trapping in the oxide due to the high channel electric field. Carriers gain kinetic energy from the lateral electric field, and some can overcome the Si/SiO₂ barrier height and cause damage at the interface between Si and SiO₂. Interface states lead to mobility degradation by scattering interaction with channel carriers. Mobility degradation leads to the drain current degradation. Charge trapping and interface state change the charge distribution above the channel and influence the threshold voltage [1]. In n-MOSFETs, the performance drifts due to HC stress could be examined via device parameters such as

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transconductance degradation and threshold voltage and mobility shift [2]. The increased random thermal motion of carriers in the channel after HC stress increases the channel thermal noise, which is a critical factor in most RF circuit design. The HC induced device degradations are correlated to the substrate current and the gate current for n-MOSFETs and p-MOSFETs, respectively. For n-MOSFETs, the correlation exists because hot carriers and $I_{sub}$ are driven by the maximum channel electric field, which occurs at the drain end of the channel. For p-MOSFETs, the charge trapping in the gate oxide is the dominant force for degradation, so the degradation is correlated with the gate current.

Gate oxide breakdown has been studied extensively. Many papers investigated the defect generation leading to breakdown and the nature of the conduction after breakdown. Recently, research on the impact of MOSFET gate oxide breakdown on circuits have been reported [3,4]. It was demonstrated that digital circuits would remain functional beyond the first gate oxide hard breakdown. RF circuits are sensitive to the parameters of their components. Therefore breakdown is reckoned to have severe impact on the performance of the circuits due to impedance mismatch and gain reduction [5]. But, big transistors are used in RF circuits; one small spot of BD path through the gate may not cause too much characteristic change. So it is worth investigating the performance of RF circuits after device BD.

**Experimental Verification**

Today’s MOS transistors are approach below 90 nm in channel length. The devices used in this work are fabricated with 160 nm CMOS technology. The oxide thickness $t_{ox}$ is 2.4 nm. The devices are tested with Cascade Probe Station, Agilent 4156B Precision Semiconductor Parameter Analyzer, and Agilent 8510C Network Analyzer. The use of device measurement stimulates students learning and triggers their curiosity and dedication. The hand on experience also provides an opportunity for students to learn beyond reading textbooks.

The oxide breakdown voltage was first determined from the Voltage Ramp Test. The gate voltage was increased from zero to 4.5 V. Then the stress condition was carefully set to a constant gate voltage $V_g = 4.5$ V and a constant drain voltage $V_d = 2$ V with the source and the substrate grounded. The stress was stopped at $I_g = 1$ mA. The overstress measurement provides students to see experimental data over a short period of time and then continue their next run of measurement. To mimic the circuit operation condition, the gate oxide stress and channel hot carrier effects are applied simultaneously. The source and body are grounded during stress. It is found that the breakdown voltage is about 3 volts. To enhance the hot electron degradation, the accelerated stress condition is set at $V_g = V_d = 2.6$ V. S-parameters of dummy pads on the same wafer are also measured and used for de-embedding the pad parasitic effects. The cutoff frequency of the device is extracted from the S-parameter measurements. Many devices were tested.

For n-channel devices, the measured threshold voltage increases with stress time because of electron trapping, and the measured mobility decreases due to the increase of interface state generation. This is verified by the degradation of the extracted parameters of BSIM3V3 models. The SBD and HC effects also degrade the RF parameters of CMOS devices. From the experimental data, S11 and S21 degrade significantly after stress, and the cutoff frequency also decreases significantly. Figure 1 shows normalized threshold voltage, mobility, drain current, transconductance, and cutoff frequency degradation versus stress time ($W = 50 \mu m$).
So far there is no systematic methodology to study RF circuit performance degradations subject to stress. More attention has been paid on device level reliability experiments. To build more reliable RF blocks, the current device level stress measurements need to be extended to RF circuit level reliability evaluations. The methodology proposed here is to combine the device level stress measurements with SpectreRF circuit simulation and circuit reliability simulation. This method is practical, accurate, and it is helpful to teach students with the design of more reliable RF circuits. The methodology is shown in Fig. 2. To evaluate HC and SBD effects on the low-noise amplifier (LNA) performance, the 0.16 \( \mu \)m NMOS device was stressed and the degraded device parameters were extracted. Using the proposed methodology, the LNA S21 degradation is shown in Fig. 3. It is clear from Fig. 3 that the LNA deviates from the matching point after stress. This is because of significant changes in the equivalent input components of the transistor such as \( C_{gs} \) and \( g_m \) that tend to degrade the input impedance matching dramatically. The gain degradation is mainly due to the decrease of the transconductance of the transistor.

![Fig. 1 Normalized parameters versus stress time](image)

**Performance Evaluation**

![Fig. 2 Methodology for design in reliability](image)
Noise figure is another important parameter for LNA. The noise figure degradation due to HC stress is shown in Fig. 4. Noise figure increases with stress.

To evaluate the gate oxide breakdown effect, an equivalent circuit accounting for gate oxide breakdown for RF applications is shown in Fig. 5. The equivalent circuit includes the intrinsic transistor, the terminal resistances ($R_g$, $R_d$, $R_s$), the substrate resistances ($R_{db}$, $R_{sh}$, $R_{dsb}$), the overlap resistances ($C_{gdo}$, $C_{gso}$), the junction capacitances ($C_{jdb}$, $C_{jsb}$), and the two inter-terminal resistances ($R_{gdb}$, $R_{gs}$). $R_g$ and the RC substrate network are included for more accurate RF modeling. The validity of the present equivalent RF circuit is verified by measured and simulated results for fresh devices before oxide breakdown as well as for those results after breakdown as shown in Fig. 6, where $W = 10 \, \mu m$, $L = 0.16 \, \mu m$, $t_{ox} = 2.4 \, nm$, $V_T = 0.4 \, V$, $R_g = 85.4 \, \Omega$, $R_d = R_s = 12.14 \, \Omega$, $R_{gdb} = 6.88 \, k\Omega$, $R_{gso} = 23 \, k\Omega$, $C_{gdo} = C_{gso} = 15.3 \, fF$, $C_{jdb} = C_{jsb} = 7 \, fF$, $R_{dsb} = 80 \, k\Omega$ and $R_{db} = R_{sh} = 49.37 \, \Omega$ are used for simulation. The model is then used to determine how the gate oxide breakdown affects RF circuits. In Fig. 6 solid squares represent fresh device measurement, empty squares represent post-breakdown measurement, thick lines represent simulation for fresh device, and thin lines represent simulation for post-breakdown device. It is clear from Fig. 6 that S-parameters degrade significantly after breakdown. After BD either a gate-to-channel or a gate-to-extension resistive path is formed. This changes the input impedance at the gate as evidenced by S11; another connection between the gate and the drain other than the original capacitive path, which explains the significant degradation of S12; and the change of the output impedance at the drain, which related to change of S22. The degradation of S21 is consistent with the decrease of $g_{in}$.
Fig. 5 Equivalent circuit including breakdown

Fig. 6 S-parameters versus frequency (magnitude and phase)
The above equivalent RF circuit after gate oxide breakdown is plugged into the Cadence Spectre simulation of an LNA. Figure 7 shows a narrow band LNA designed at 1.8 GHz. A cascode structure is used to minimize the Miller effect and increase the gain. Source inductive degeneration is adopted to improve linearity. The inductance at the drain of the cascode device creates a resonant load with the input capacitance of the following mixer stage. Both the input device M1 and the cascode device M2 are composed of 20 fingers with each being 10 µm wide. It is worth mentioning that not all fingers experience breakdown simultaneously. Noise figures of the LNA after up to two fingers of M1 break down is shown in Fig. 8. The noise figure increases more drastically after 2 fingers of M1 break. The circuit performance degradation can be explained by the following. After BD a leakage path exists across the gate oxide. This adds another noise source to the transistor, thus degrades the NF. Also the significant increase in gate current significantly increases the real part of the complex input impedance. The immediate impact of such a change is to destroy the impedance matching condition, which is critical for LNA performance. Thus, circuit's S-parameters degrade significantly and potentially become unacceptable.

Fig. 7 A low-noise amplifier

Fig. 8 Noise figure versus frequency
In order to reduce the HC effects on RF circuits, two techniques are proposed in this section. The first technique is to use a cascode structure. HC effect is caused by high voltage drop between the drain and source of the transistors in the circuits. If the drain voltage is reduced, the HC effect is expected to reduce. The Cascode structure can achieve this goal. SBD effect can be reduced by decreasing the voltage swings.

**Summary**

Traditional textbooks do not cover CMOS reliability for the design of RF circuits using today’s nanoelectronics technology. For effective learning, students first need to know how hot electrons and gate gate oxide breakdown occur. The experimental data of stressed devices are then demonstrated for further understanding. Using stressed transistors data and RF device model, RF circuit performances subject to stress are examined. Hot carrier effect and gate oxide breakdown increase noise figure and decrease power gain of MOS transistor circuits. From physical insight into RF circuit degradation, one can design RF circuits to reduce hot electron and oxide breakdown effects on circuit performance. This flow provides a robust circuit design and is essential in today’s wireless integrated circuit design and education.

**References**

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J.S. Yuan received both the M.S. and Ph.D. degrees (1984 and 1988) from the University of Florida. He joined the faculty at the University of Central Florida (UCF) in 1990 after one year of industrial experience at Texas Instruments, Inc., where he was involved with the 16-MB CMOS DRAM design. Currently, he is a professor and director of the Chip Design and Reliability Laboratory at the Department of Electrical Engineering at UCF.


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